Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claim 1-121. (canceled)

122. (currently amended) A circuitry ~~An electronic~~ component comprising:

a first intra-chip driver or receiver; ~~multiple I/O circuits;~~

a second intra-chip driver or receiver;

~~an~~ a first metallization ~~interconnecting~~ structure;

a passivation layer over said first metallization ~~interconnecting~~ structure; and

~~an upper~~ a second metallization ~~interconnecting~~ structure over said passivation layer, wherein said second metallization structure connects said first intra-chip driver or receiver and said second intra-chip driver or receiver. ~~and connecting said multiple I/O circuits.~~

123. (currently amended) The circuitry ~~electronic~~ component of Claim 122, wherein said passivation layer comprises a topmost nitride layer of said circuitry component.

124. (currently amended) The circuitry ~~electronic~~ component of Claim 122, wherein said passivation layer comprises a topmost oxide layer of said circuitry component.

125. (currently amended) The circuitry ~~electronic~~ component of Claim 122, wherein said passivation layer comprises a topmost CVD insulating layer of said circuitry component.

Claim 126. (canceled)

127. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit address signals.

128. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit data signals.

129. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit logic signals.

130. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit analog signals.

131. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second interconnecting structure ~~signal bus~~ is used to transmit clock signals.

132. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit a power voltage.

133. (currently amended) The circuitry ~~electronic~~ component of Claim 122, ~~126,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit a ground voltage.

134. (currently amended) The circuitry ~~electronic~~ component of Claim 122 further comprising an off-chip driver, receiver or I/O circuit and an external connection, wherein said external connection is connected to said off-chip driver, receiver or I/O circuit, and said second metallization structure connects said off-chip driver, receiver or I/O circuit, said first intra-chip driver or receiver, and said second intra-chip driver or receiver. ~~one of said multiple I/O circuits.~~

135. (currently amended) The circuitry ~~electronic~~ component of Claim 134 further comprising an ESD circuit connected to said external connection.

136. (currently amended) The circuitry ~~electronic~~ component of Claim 122 is a semiconductor chip.

137. (currently amended) The circuitry ~~electronic~~ component of Claim 122 is a semiconductor wafer.

138. (currently amended) The circuitry ~~electronic~~ component of Claim 122, wherein said second metallization structure is used to transmit a signal output from a voltage regulator. ~~said multiple I/O circuits comprise a receiver.~~

Claim 139. (canceled)

140. (currently amended) A circuitry ~~An electronic~~ component comprising:

a semiconductor circuit;

an intra-chip driver or receiver; ~~a first I/O circuit;~~

an off-chip driver, receiver or I/O circuit; ~~a second I/O circuit;~~

a first metallization ~~an interconnecting~~ structure connecting said semiconductor circuit and said intra-chip driver or receiver; ~~first I/O circuit;~~

an external connection connected to said off-chip driver, receiver or I/O circuit;

a passivation layer over said first metallization ~~interconnecting~~ structure; and

a second metallization ~~an upper interconnecting~~ structure over said passivation layer, wherein said second metallization structure connects ~~and connecting~~ said intra-chip driver or receiver and said off-chip driver, receiver or I/O circuit. ~~first and second I/O circuits.~~

141. (currently amended) The circuitry ~~electronic~~ component of Claim 140, wherein said passivation layer comprises a topmost nitride layer of said circuitry component.

142. (currently amended) The circuitry ~~electronic~~ component of Claim 140, wherein said passivation layer comprises a topmost oxide layer of said circuitry component.

143. (currently amended) The circuitry ~~electronic~~ component of Claim 140, wherein said passivation layer comprises a topmost CVD insulating layer of said circuitry component.

Claim 144. (canceled)

145. (currently amended) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit address signals.

146. (currently amended) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit data signals.

147. (currently amended) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit logic signals.

148. (new) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit analog signals.

149. (currently amended) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit clock signals.

150. (currently amended) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit a power voltage.

151. (currently amended) The circuitry ~~electronic~~ component of Claim 140, ~~144,~~ wherein said second metallization structure ~~signal bus~~ is used to transmit a ground voltage.

Claim 152. (canceled)

153. (currently amended) The circuitry ~~electronic~~ component of Claim 140 ~~152~~ further comprising an ESD circuit connected to said external connection.

154. (currently amended) The circuitry ~~electronic~~ component of Claim 140 is a semiconductor chip.

155. (currently amended) The circuitry ~~electronic~~ component of Claim 140 is a semiconductor wafer.

156. (currently amended) The circuitry ~~electronic~~ component of Claim 140, wherein said second metallization structure is used to transmit a signal output from a voltage regulator. ~~said first I/O circuit comprises a receiver.~~

Claims 157-159. (canceled)

160. (currently amended) A method of fabricating an electronic component, comprising:

providing a semiconductor wafer comprising a first intra-chip driver or receiver, a second intra-chip driver or receiver, ~~multiple I/O circuits,~~ a first metallization ~~an interconnecting~~ structure and a passivation layer, said passivation layer being over said first metallization ~~interconnecting~~ structure; and

forming a second metallization ~~an upper interconnecting~~ structure over said passivation layer, wherein said second ~~upper~~ interconnecting structure connects said first intra-chip driver or receiver and said second intra-chip driver or receiver. ~~multiple I/O circuits.~~

161. (currently amended) The method of Claim 160, wherein said passivation layer comprises a ~~topmost~~ nitride layer.

162. (currently amended) The method of Claim 160, wherein said passivation layer comprises ~~a topmost~~ an oxide layer.

163. (currently amended) The method of Claim 160, wherein said passivation layer comprises ~~a topmost~~ an insulating layer formed using a CVD process.

164. (currently amended) The method of Claim 160, wherein said forming said second metallization structure comprises electroplating. ~~multiple I/O circuits comprise a receiver.~~

165. (currently amended) The method of Claim 160, wherein said forming said second metallization structure comprises sputtering. ~~multiple I/O circuits comprise a driver.~~

166. (currently amended) A method of fabricating an electronic component, comprising:

providing a semiconductor wafer comprising a semiconductor circuit, an intra-chip driver or receiver, an off-chip driver, receiver or I/O circuit, ~~a first I/O circuit, a second I/O circuit,~~ a first metallization ~~an interconnecting~~ structure, an external connection and a passivation layer, said first metallization ~~interconnecting~~ structure connecting said intra-chip driver or receiver ~~first I/O circuit~~ and said semiconductor circuit, said external connection being connected to said off-chip driver, receiver or I/O circuit, and said passivation layer being over said first metallization ~~interconnecting~~ structure; and

forming a second metallization ~~an upper interconnecting~~ structure over said passivation layer, wherein said second metallization ~~upper interconnecting~~ structure connects said intra-chip driver or receiver and said off-chip driver, receiver or I/O circuit. ~~first and second I/O circuits.~~

167. (currently amended) The method of Claim 166, wherein said passivation layer comprises a ~~topmost~~ nitride layer.

168. (currently amended) The method of Claim 166, wherein said passivation layer comprises ~~a topmost~~ an oxide layer.

169. (currently amended) The method of Claim 166, wherein said passivation layer comprises ~~a topmost~~ an insulating layer formed using a CVD process.

170. (currently amended) The method of Claim 166, wherein said forming said second metallization structure comprises electroplating. ~~multiple I/O circuits comprise a receiver.~~

171. (currently amended) The method of Claim 166, wherein said forming said second metallization structure comprises sputtering. ~~multiple I/O circuits comprise a driver.~~